PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Nathan R. Brown

Serial No.: 10/715,267

Filed: November 17, 2003

For: METHODS FOR POLISHING SEMICONDUCTOR DEVICE STRUCTURES BY DIFFERENTIALLY APPLYING PRESSURE TO SUBSTRATES THAT CARRY THE SEMICONDUCTOR DEVICE STRUCTURES

Confirmation No.: 4590

Examiner: S. Macarthur

Group Art Unit: 1763

Attorney Docket No.: 2269-4375.1US

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EV827470296US

Date of Deposit with USPS: October 3, 2006

Person making Deposit: Brick G. Power

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sir:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

10/06/2006 YPOLITE1 00000042 201469 10715267
01 FC:1402 500.00 OP

(I) REAL PARTY IN INTEREST

U.S. Application Serial No. 10/715,267 (hereinafter "the '267 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 012267, Frame No. 0959. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

(II) RELATED APPEALS AND INTERFERENCES

There are no related appeals, interferences, or other actions of which appellants or their attorneys are aware that may have a bearing on the outcome of the decision of the Board of Patent Appeals and Interferences (hereinafter "the Board") in the above-referenced appeal.

(III) STATUS OF CLAIMS

There are currently thirty (30) claims, numbered 1 and 3-31, pending and under consideration in the '267 Application. All thirty claims stand finally rejected. The final rejections of the claims of the '267 Application are being appealed.

(IV) STATUS OF AMENDMENTS

The most recent claim amendments the '267 Application were introduced in an Amendment that was filed on January 11, 2006.

A Notice of Appeal was filed in the '267 Application on July 3, 2006, and is followed by this Appeal Brief. This Appeal Brief is being submitted with a petition for a one month extension of time and the appropriate fee.

(V) SUMMARY OF CLAIMED SUBJECT MATTER

The '267 Application includes claims that recite methods that include biasing independently movable pressurization structures to selectively apply a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure. Independent claim 1; paragraphs **[0010]** and **[0054]**.

In addition, the '267 Application includes claims that are directed to methods that include "selectively applying [pressure] at locations beneath areas of . . . at least one second semiconductor device structure that correspond to . . . raised areas of [a] first semiconductor device structure . . ." Independent claim 16; paragraphs **[0010]** and **[0056]**. The raised areas of the first semiconductor device structure may be located by employing metrology techniques. Claim 17; paragraph **[0055]**. A sufficient amount of pressure may be applied at each location of the second semiconductor device structure that corresponds to a raised area on the first semiconductor device structure to form a substantially planar surface the second semiconductor device structure. Claim 18; paragraphs **[0010]** and **[0056]**. Further, different amounts of pressure may be selectively applied to different locations that correspond to raised areas. Claim 19; paragraphs **[0010]** and **[0056]**. The amount of pressure applied to each location of the semiconductor device structure may correspond to a height of a corresponding raised area of the first semiconductor device structure. Claim 20; paragraphs **[0010]** and **[0056]**.

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The rejections of claims 1 and 6-15 under 35 U.S.C. § 102(e) for reciting subject matter that is allegedly anticipated by the subject matter described in U.S. Patent 6,623,343 to Kajiwara et al. (hereinafter "Kajiwara");

(B) The 35 U.S.C. § 103(a) rejections of claims 3-5 for being drawn to subject matter that is assertedly unpatentable over the subject matter taught in Kajiwara, in view of teachings from U.S. Patent 6,436,828 to Chen et al. (hereinafter "Chen"); and

(C) The rejections of claims 16-31 under 35 U.S.C. § 103(a) for being directed to subject matter which is purportedly unpatentable over the teachings of U.S. Patent 6,561,871 to Sommer (hereinafter "Sommer") or Chen, in view of teachings from U.S. Patent 6,594,542 to Williams (hereinafter "Williams").

(VII) ARGUMENT

(A) CLAIM REJECTIONS UNDER 35 U.S.C. § 102

Claims 1 and 6-15 are rejected under 35 U.S.C. § 102(e) for reciting subject matter that is allegedly anticipated by the subject matter described in Kajiwara.

(1) LEGAL AUTHORITY

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053

(Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

(2) ART RELIED UPON

Kajiwara

Kajiwara describes an apparatus that includes concentric tubular pressure rings or bladders 255 that may be independently inflated and pressurized. The bladders 255 are configured to individually apply pressure to a membrane 250 that, in turn, applies pressure to a wafer 230.

(3) ANALYSIS

The bladders 255 of the apparatus of Kajiwara are not independently movable, as would be required for Kajiwara to expressly or inherently describe each and every element of independent claim 1; instead, they are independently inflatable and pressurizable. When pressurized, they remain in place as air or gases are introduced therein.

Moreover, the bladders 255 of the apparatus of Kajiwara do not individually apply pressure to a surface of a semiconductor device structure. The membrane 250, which includes a surface 256 that contacts the entire back side 244 of the wafer 230, applies pressure from any combination of the bladders 255 to the back side 244 of the wafer 230. Further, the bladder 250 spreads the pressure applied thereto by any one bladder 255. When multiple bladders 255 apply pressure to the membrane 250, the membrane 250 will inherently even out the pressure applied thereto, in a gradient-type fashion. This characteristic of a membrane of the type described in

Kajiwara prevents the bladders 255 from individually applying pressure to a major surface of a semiconductor device structure.

Therefore, Kajiwara does not expressly or inherently describe a method that includes biasing independently movable pressurization structures to selectively apply a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure, as recited in independent claim 1.

Claims 6-15 are each allowable, among other reasons, for depending from claim 1, which is allowable.

Reversal of the 35 U.S.C. § 102(e) rejections of claims 1 and 6-15 is respectfully requested.

(B) CLAIM REJECTIONS UNDER 35 U.S.C. § 103(A)

Claims 3-5 and 16-31 have been rejected under 35 U.S.C. § 103(a).

(1) LEGAL AUTHORITY

The standard for establishing, maintaining, and upholding a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

> limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant=s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(2) ADDITIONAL ART RELIED UPON

Chen

Chen teaches a polishing apparatus that includes magnets for controlling the pressure applied to different portions of a substrate. Col. 2, lines 47-52. The apparatus includes a carrier head 100 that supports a flexible membrane 104, or circular sheet. Col. 4, lines 26-32, 45-48; FIG. 2. The flexible membrane 104 includes magnetically sensitive particles distributed therethrough. *Id.* The carrier head 100 also includes three coils, 108, 110, and 112, that are coupled to voltage sources 140, 142, and 144. Col. 4, lines 28-31; col. 5, lines 38-42; FIG. 2. The voltage applied to a coil creates an electrical current, which in turn induces a magnetic field proportional in intensity to the current flowing through the coil. Col. 5, lines 42-46. The carrier head 100 also includes a loading chamber 120 that applies a downward load to the membrane 104. Col. 4, lines 63-67; FIG. 2.

In application, the electric current flowing through the coils 108, 110, and 112 induces a magnetic field that interacts with the magnetic particles 118 in the membrane 104. The magnetic field "create[s] a primary field region in a ...first region of the flexible membrane [104] and a secondary field region ...in a second region of the flexible membrane..." Col. 5, lines 49-55. As an example, activating the third coil 112 "will apply the primary magnetic field to at least the central, intermediate and outer membrane portions 132, 134 and 136." Col. 5, lines 65-67; FIG. 2.

Sommer

Sommer teaches a linear drive mechanism for chemical-mechanical planarization. Col. 3, lines 53-56. A substrate carrier 402 carries a substrate (not shown) against a polishing surface of a CMP apparatus. Col. 12, lines 8-11; FIG. 11. The carrier plate 402 has several magnets 420, 422, 424, and 426 that facilitate incremental movement of the carrier plate 402 in the X and Y directions (*see, e.g.,* U.S. Patent 3,376,578 referenced and incorporated into Sommer) while providing an attractive force F in the Z direction between the carrier plate 402 and the polishing plate 406. Col. 28-30; FIGS. 11, 13. Alternatively, the magnets 520, 522, 524, and 526 may be permanently mounted in the platen 531. Col. 15, lines 47-53; FIG. 15.

Williams

The teachings of Williams relate to a method for controlling material removal rates during chemical-mechanical polishing (CMP) processes. Col. 1, lines 15-19. The method of Williams compensates for inconsistencies in a polishing pad over time, from wafer-to-wafer. Col. 5, lines 17-20. In the method of Williams, the thickness of a wafer 102 is measured prior to polishing a material layer, or film, on the wafer. Col. 6, lines 18-20; FIG. 6. A polishing apparatus 200 polishes the material layer for a predetermined time, during which the pressure "applied by the wafer 102 against the polishing surface 206 is measured and controlled through sensors" on the polishing apparatus. Col. 6, lines 41-47; FIG. 6. After polishing for the predetermined time, an "after polishing" thickness measurement of the wafer 102 is made. Col. 6, lines 53-55. The "before" and "after" thickness measurements are used to calculate a

linear estimation factor based on the material removal rate, which is used to adjust the polishing time. Col. 6, lines 55-60. The calculated linear estimation factor, which is based on the measured material removal rates of one or more prior acts of polishing, is used to adjust the durations for which other wafers are subsequently polished so that the polishing pad may be used to remove the same thickness of material from the other wafers. Col. 6, lines 59-62.

(3) ANALYSIS

(a) KAJIWARA IN VIEW OF CHEN

Claims 3-5 stand rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is assertedly unpatentable over the subject matter taught in Kajiwara, in view of teachings from Chen.

Claims 3-5 are allowable, among other reasons, for depending from claim 1, which is allowable.

It is also respectfully submitted that each of claims 3-5 is allowable because the Office has not established a *prima facie* case of obviousness against them.

As noted above, Kajiwara does not teach or suggest biasing independently movable pressurization structures against the backside of a semiconductor device structure. Rather, the effects of inflating a bladder are spread out across a single membrane 250 that interacts with the backside of a wafer.

As Chen teaches that activation of one coil 112 "will apply the primary magnetic field to at least the central, intermediate and outer . . . portions 132, 134 and 136" of a membrane 104 (col. 5, lines 65-67; FIG. 2), it is apparent that magnetic fields that are generated in accordance

with the method of Chen act across the entire membrane 104 such that an effect on one region of the membrane 104 (e.g., 132, 134, and 136) is at least partially translated to adjacent regions of the membrane 104. This interdependence is further illustrated in FIG. 4 of Chen, which is a graph of the removal rate of a material at various radial positions of a substrate under differing magnetic fields. Col. 6, lines 32-67; col. 7, lines 1-15; FIG. 4.

As the effect of the application of a magnetic field to a particular location of a membrane is spread to other regions of the membrane, which is in turn the only feature of the apparatus of Chen that is biased against a surface of a substrate, Chen cannot be considered to teach or suggest biasing independently movable pressurization structures against the backside of a semiconductor device structure.

Therefore, it is respectfully submitted that Kajiwara and Chen, taken either separately or together, do not teach or suggest each and every element of independent claim 1, from which claims 3-5 depend. Moreover, it is respectfully submitted that, in view of the fact that neither Kajiwara nor Chen teaches or suggests an apparatus that includes elements that individually apply pressure to corresponding regions of a semiconductor substrate, one of ordinary skill in the art wouldn't have been motivated to combine the teachings of these references in the asserted manner, or had any reason to expect that their combination in the asserted manner would have been successful.

Rather, it appears that any such motivation could only have been improperly gleaned by the Examiner from the subject matter recited in the claims of the above-referenced application.

As a *prima facie* case of obviousness has not been established, it is respectfully submitted that, under 35 U.S.C. § 103(a), each of claims 3-5 is drawn to subject matter that is allowable over the teachings of Kajiwara and Chen.

(b) SOMMER OR CHEN IN VIEW OF WILLIAMS

Claims 16-31 stand rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is purportedly unpatentable over the teachings of Sommer or Chen, in view of teachings from Williams.

It is respectfully submitted that there are several reasons that teachings from Sommer or Chen, in view of the teachings of Williams, do not support a *prima facie* case of obviousness against any of claims 16-31.

First, it is respectfully submitted that none of Sommer, Chen, or Williams, taken separately or in any combination, teaches or suggests each and every claim element. Specifically, with respect to the method of independent claim 16, none of Sommer, Chen, or Williams teaches or suggests a method that includes "selectively applying [pressure] at locations beneath areas of . . . at least one second semiconductor device structure that correspond to . . . raised areas of [a] first semiconductor device structure . . ." Rather, the teachings of Sommer are limited to polishing apparatus that are configured to move substrates linearly, while Chen teaches methods for applying pressure gradients to semiconductor wafers through membranes, and Williams merely teaches methods for adjusting polishing times as polishing pads become less effective.

Second, it is respectfully submitted that, without the benefit of hindsight that the claims of the above-referenced application afford to the Office, one of ordinary skill in the art wouldn't

have been motivated to combine teachings from Sommer or Chen with teachings from Williams in the asserted manner. In particular, the teachings of Sommer relate to polishing apparatus with magnets that facilitate incremental movement of a substrate carrier 402 relative to a polishing pad without selectively applying pressure to different locations of a semiconductor device structure, let alone selectively applying pressure in response to the locations of raised areas on a previously polished semiconductor device structure of the same type. Chen teaches a method for applying a pressure gradient to a surface of a semiconductor device structure, but does not teach or suggest doing so in response to raised areas of a previously polished semiconductor device structure of the same type. The teachings of Williams are limited to monitoring for the sake of making adjustments in polishing times as a polishing pad becomes worn or otherwise less effective. None of these references would have provided one of ordinary skill in the art with any motivation to combine their teachings in such a way as to, in response to raised areas noted following polishing of a first semiconductor device structure, selectively apply pressure to at least one second semiconductor device structure of the same type.

Third, it is respectfully submitted that, since none of Sommer, Chen, or Williams teaches or suggests evaluating raised areas of a first semiconductor device following polishing thereof, then using that information to improve the planarity of subsequently polished semiconductor devices of the same type, one of ordinary skill in the art wouldn't have had any reason to expect that the teachings of Sommer or Chen could have been successfully combined with teachings from Williams in the asserted manner.

Therefore, no combination of teachings from Sommer, Chen, or Williams supports a *prima facie* case of obviousness against independent claim 16 under 35 U.S.C. § 103(a). As

such, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 16 is allowable over the subject matter taught in Chen, Sommer, and Williams.

Each of claims 17-31 is allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

Claim 17 is additionally allowable because none of Chen, Sommer, or Williams teaches or suggests a method that includes employing metrology techniques to locate raised areas.

Claim 18 is additionally allowable because none of Chen, Sommer, or Williams teaches or suggests a method that includes applying a sufficient amount of pressure at each of the locations that corresponds to a raised area to form a substantially planar surface on the at least one second semiconductor device structure.

Claim 19 is additionally allowable because none of Chen, Sommer, or Williams teaches or suggests a method that includes selectively applying different amounts of pressure at different locations that correspond to raised areas.

Claim 20 is additionally allowable because none of Chen, Sommer, or Williams teaches or suggests a method that includes determining an appropriate amount of pressure to apply to each of the locations based on a height of each corresponding raised area.

Claim 25 is additionally allowable because none of Chen, Sommer, or Williams teaches or suggests a method that includes biasing at least one pressurization structure against the backside of the at least one second semiconductor device structure after a first semiconductor device structure has been polished and any raised areas thereon have been located.

Reversal of the 35 U.S.C. § 103(a) rejections of claims 16-31 is respectfully requested.

(VIII) CLAIMS APPENDIX

Each claim that has been finally rejected in the '267 Application is set forth in CLAIMS APPENDIX to this Appeal Brief.

(IX) EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

(X) RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

(XI) CONCLUSION

It is respectfully submitted that:

(A) Claims 1 and 6-15 are allowable under 35 U.S.C. § 102(e) for reciting subject matter that is novel over the subject matter described in Kajiwara;

(B) Claims 3-5 are allowable under 35 U.S.C. § 103(a) being drawn to subject matter that is patentable over the subject matter taught in Kajiwara, in view of teachings from Chen; and

(C) Claims 16-31 are allowable under 35 U.S.C. § 103(a) for being directed to subject matter which is patentable over the teachings of Sommer or Chen, in view of teachings from Williams.

Accordingly, it is respectfully requested that the rejections of claims 1-31 be reversed, and that each of these claims be allowed.

Respectfully submitted,

Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: September 27, 2006
BGP/eg
Document in ProLaw

CLAIMS APPENDIX

1. A method for polishing or planarizing a surface of a semiconductor device structure, comprising:

biasing independently movable pressurization structures to selectively apply a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure; and

polishing or planarizing at least one layer on the surface of the semiconductor device structure.

3. The method of claim 1, wherein biasing comprises magnetically biasing at least one of the independently movable pressurization structures against the backside.

4. The method of claim 3, wherein magnetically biasing comprises magnetically repelling at least one of the independently movable pressurization structures toward the backside.

5. The method of claim 3, wherein magnetically biasing comprises magnetically attracting at least one of the independently movable pressurization structures toward the backside.

6. The method of claim 1, wherein biasing comprises resiliently biasing at least one of the independently movable pressurization structures against the backside.

7. The method of claim 6, wherein selectively applying comprises selectively applying a negative pressure to at least one of the independently movable pressurization structures.

8. The method of claim 1, wherein biasing comprises applying a positive pressure to at least one of the independently movable pressurization structures.

9. The method of claim 1, wherein polishing or planarizing comprises chemical-mechanical polishing.

10. The method of claim 1, wherein biasing and polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure.

11. The method of claim 1, further comprising locating at least one raised area on an active surface of the semiconductor device structure.

12. The method of claim 11, wherein selectively applying a plurality of different amounts of pressure comprises applying an appropriate amount of pressure to the backside of the semiconductor device structure, opposite the at least one raised area so as to planarize the active surface during the polishing or planarizing.

13. The method of claim 11, wherein selectively applying a plurality of different amounts of pressure comprises selectively applying pressure to a backside of another semiconductor device structure of the same type as the semiconductor device structure, opposite a location of the at least one raised area of the semiconductor device structure.

14. The method of claim 13, wherein polishing or planarizing comprises forming a substantially planar surface on the another semiconductor device structure.

15. The method of claim 1, comprising substantially simultaneously applying the plurality of different amounts of pressure to the backside of the semiconductor device structure.

16. A method for polishing at least one layer on a semiconductor device structure, comprising:

polishing at least one layer of a first semiconductor device structure;

locating any raised areas on the first semiconductor device structure following the polishing;

selectively applying pressure to a backside of at least one second semiconductor device structure of a same type as the first semiconductor device structure, the selectively applying being effected at locations beneath areas of the at least one second semiconductor device structure that correspond to the raised areas of the first semiconductor device structure; and

at least mechanically polishing at least one layer of the at least one second semiconductor device structure.

17. The method of claim 16, wherein locating comprises employing metrology techniques.

18. The method of claim 16, wherein selectively applying comprises applying a sufficient amount of pressure at each of the locations to form a substantially planar surface on the at least one second semiconductor device structure.

19. The method of claim 16, wherein selectively applying comprises selectively applying different amounts of pressure at different ones of the locations.

20. The method of claim 16, wherein selectively applying comprises determining an appropriate amount of pressure to apply to each of the locations based on a height of each corresponding raised area.

21. The method of claim 16, wherein selectively applying comprises selectively applying pressure to the backside of the at least one second semiconductor device structure to at least one annular location.

22. The method of claim 16, wherein polishing comprises mechanically polishing the at least one layer of the first semiconductor device structure.

23. The method of claim 16, wherein polishing comprises chemical-mechanical polishing the at least one layer of the first semiconductor device structure.

24. The method of claim 16, wherein at least mechanically polishing comprises chemical-mechanical polishing the at least one layer of the at least one second semiconductor device structure.

25. The method of claim 16, wherein selectively applying comprises biasing at least one pressurization structure against the backside of the at least one second semiconductor device structure.

26. The method of claim 25, wherein biasing comprises employing a magnet to bias the at least one pressurization structure against the backside.

27. The method of claim 26, wherein employing the magnet comprises repelling the at least one pressurization structure toward the backside to effect biasing.

28. The method of claim 26, wherein employing the magnet comprises attracting the at least one pressurization structure toward the backside to effect biasing.

29. The method of claim 25, wherein biasing comprises resiliently biasing the at least one pressurization structure against the backside.

30. The method of claim 29, wherein selectively applying further comprises applying a negative pressure to the at least one pressurization structure.

31. The method of claim 25, wherein biasing comprises applying a selected amount of positive pressure to the at least one pressurization structure.